AMENDMENTS TO THE CLAIMS

Please enter the following amendments:

1. (Currently Amended) A programmable processor comprising:

an instruction path;

a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a register file operable to receive and store data from the data path and communicate the stored data to the data path; and

an execution unit coupled to the instruction and data paths and operable to decode and execute instructions received from the instruction path, wherein in response to decoding a single instruction for writing data to memory based on a mask and data contained in at least one register, the mask consisting of N independently selectable mask bits, N being an integer multiple of eight, each of the mask bits corresponding to a data bit contained in the at least one register ~~comprising a plurality of mask fields that each corresponds to a data field of the data contained in the at least one register~~, each of the ~~plurality of mask fields~~ mask bits being independently selectable as either a write-enabled ~~mask field~~ mask bit or a write-disabled ~~mask field~~ mask bit, the execution unit is operable to:

(i) detect some of the ~~mask fields~~ mask bits of the mask as being selected as write-enabled ~~mask fields~~ mask bits to identify corresponding ~~data fields~~ data bits of the data contained in the at least one register as write-enabled ~~data fields~~ data bits; and

(ii) cause the write-enabled ~~data fields~~ data bits to be written to a specified memory location.

2. (Canceled)

3. (Canceled)

4. (Currently Amended) The processor of claim 1 wherein the execution unit is operable to cause the write-enabled ~~data fields~~ data bits to be written to the specified memory location by reading an unaltered field of data from the specified memory location and writing the unaltered field of data along with the write-enabled ~~data fields~~ data bits to the specified memory location.

5. (Original) The processor of claim 1 wherein the mask is contained in a specified register.

6. (Previously Presented) The processor of claim 1 wherein the memory location is specified by a register.

7. (Original) The processor of claim 1 wherein the specified memory location comprises a section of memory having a specific width and beginning at a specific memory address.

8. (Currently Amended) The processor of claim 1 wherein each write-enabled ~~mask field~~ mask bit is indicated as a logic 1.

9. (Previously Presented) The processor of claim 1 wherein the execution unit is further operable to, in response to decoding a second single instruction specifying a register containing a first plurality of floating-point operands and another register containing a second plurality of floating-point operands, multiply the first plurality of floating-point operands by the second plurality of floating-point operands to produce a plurality of products and provide the plurality of products to partitioned fields of a result register as a catenated result.

10. (Currently Amended) A data processing system comprising:

(a) a bus coupling components in the data processing system;

(b) an external memory coupled to the bus;

(c) a programmable microprocessor coupled to the bus and capable of operation independent of another host processor, the microprocessor comprising:

an instruction path; a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a register file operable to receive and store data from the data path and communicate the stored data to the data path; and

an execution unit coupled to the instruction and data paths and operable to decode and execute instructions received from the instruction path, wherein in response to decoding a single instruction for writing data to memory based on a mask and data contained in at least one register, the mask consisting of N independently selectable mask bits, N being an integer multiple of eight, each of the mask bits corresponding to a data bit contained in the at least one register ~~comprising a plurality of mask fields that each corresponds to a data field of the data~~

~~contained in the at least one register~~, each of the ~~plurality of mask fields~~ mask bits being independently selectable as either a write-enabled ~~mask field~~ mask bit or a write-disabled ~~mask field~~ mask bit, the execution unit is operable to:

(i) detect some of the ~~fields~~ mask bits of the mask as being selected as write-enabled ~~mask fields~~ mask bits to identify corresponding ~~data fields~~ data bits of the data contained in the at least one register as write-enabled ~~data fields~~ data bits; and

(ii) cause the write-enabled ~~data fields~~ data bits to be written to a specified memory location.

11. (Canceled)

12. (Canceled)

13. (Currently Amended) The system of claim 10 wherein the execution unit is operable to cause the write-enabled ~~data fields~~ data bits to be written to the specified memory location by reading an unaltered field of data from the specified memory location and writing the unaltered field of data along with the write-enabled ~~data fields~~ data bits to the specified memory location.

14. (Original) The system of claim 10 wherein the mask is contained in a specified register.

15. (Previously Presented) The system of claim 10 wherein the memory location is specified by a register.

16. (Original) The system of claim 10 wherein the specified memory location comprises a section of memory having a specific width and beginning at a specific memory address.

17. (Currently Amended) The system of claim 10 wherein each write-enabled ~~mask field~~ mask bit is indicated as a logic 1.

18. (Previously Presented) The system of claim 10 wherein the execution unit is further operable to, in response to decoding a second single instruction specifying a register containing a first plurality of floating-point operands and another register containing a second plurality of floating-point operands, multiply the first plurality of floating-point operands by the second plurality of floating-point operands to produce a plurality of products and provide the plurality of products to partitioned fields of a result register as a catenated result.

19. (Currently Amended) A programmable processor comprising:

a virtual memory addressing unit;

an instruction path and a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a cache operable to retain data communicated between the external interface and the data path;

a register file comprising a plurality of registers coupled to the data path; and an execution unit, coupled to the instruction and data paths, that is operable to decode and execute instructions received from the instruction path, the execution unit capable of performing a bitwise insert operation that operates on a first and a second operand stored in at least one register in the register file, the second operand consisting of N independently selectable bits, N being an integer multiple of eight, wherein each bit in the second operand is ~~individually~~ independently selectable as either having a first predetermined value or a second predetermined value, wherein for each bit in the first operand, the bitwise insert operation inserts the bit into a corresponding bit position in a destination value if a corresponding bit ~~from~~ in the second operand has a the first predetermined value.

20. (Previously Presented) The programmable processor of claim 19 wherein the first predetermined value is a logic 1.

21. (Previously Presented) The programmable processor of claim 19 wherein for each bit in the first operand, the bitwise insert operation maintains a corresponding bit position in the destination value as unchanged if a corresponding bit in the second operand has the second predetermined value.

22. (Previously Presented) The programmable processor of claim 21 wherein the second predetermined value is a logic 0.

23. (Previously Presented) The programmable processor of claim 19 wherein the bitwise insert operation stores the destination value into memory.

24. (Previously Presented) The programmable processor of claim 19 wherein each of the first and second operands has a width of 64 bits.

25. (Previously Presented) The programmable processor of claim 19 wherein the execution unit is further capable of executing a plurality of different group floating-point arithmetic operations that arithmetically operate on multiple floating-point operands stored in partitioned fields of registers in the register file to produce a catenated result that is returned to a register in the register file, wherein the catenated result comprises a plurality of individual floating-point results.

26. (Currently Amended) A device having installed therein a programmable processor, the programmable processor comprising:

a virtual memory addressing unit;

an instruction path and a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a cache operable to retain data communicated between the external interface and the data path;

a register file comprising a plurality of registers coupled to the data path; and an execution unit, coupled to the instruction and data paths, that is operable to decode and execute instructions received from the instruction path, the execution unit capable of performing a bitwise insert operation that operates on a first and a second operand stored in at least one register in the register file, the second operand consisting of N independently selectable bits, N being an integer multiple of eight, wherein each bit in the second operand is ~~individually~~ independently selectable as either having a first predetermined value or a second predetermined value, wherein for each bit in the first operand, the bitwise insert operation inserts the bit into a corresponding bit position in a destination value if a corresponding bit in the second operand has the first predetermined value.

27. (Previously Presented) The device of claim 26 wherein the first predetermined value is a logic 1.

28. (Previously Presented) The device of claim 26 wherein for each bit in the first operand, the bitwise insert operation maintains a corresponding bit position in the destination value as unchanged if a corresponding bit in the second operand has the second predetermined value.

29. (Previously Presented) The device of claim 28 wherein the second predetermined value is a logic 0.

30. (Previously Presented) The device of claim 26 wherein the bitwise insert operation stores the destination value into memory.

31. (Previously Presented) The device of claim 26 wherein each of the first and second operands has a width of 64 bits.

32. (Previously Presented) The device of claim 26 wherein the execution unit is further capable of executing a plurality of different group floating-point arithmetic operations that arithmetically operate on multiple floating-point operands stored in partitioned fields of registers in the register file to produce a catenated result that is returned to a register in the register file, wherein the catenated result comprises a plurality of individual floating-point results.